Amendment to the Drawings:

The attached sheets of drawings include changes to Figs. 1, 3A and 4. These sheets, which include Figs. 1, 3A and 4, replace the original sheets including Figs. 1, 3A and 4. In Fig. 1, previously omitted connection-line connected between the shift register 11 and the test signal input terminal 12, and previously omitted connection-lines connected among the shift register 103, the data register 104, the level shifter 105 and the multiplexer 106 and the output circuit 107, had been added.

As well as the amendment to Fig. 1, in Fig. 3A, previously omitted connection-line connected between the shift register 211 and the test signal input terminal 212, and previously omitted connection-lines connected among the shift register 103, the data register 104, the level shifter 105 and the multiplexer 106 and the output circuit 107, had been added. Furthermore, As well as the amendment to Figs. 1 and 3A, in Fig. 4, previously omitted connection-line connected between the shift register 311 and the test signal input terminal 312, and previously omitted connection-lines connected among the shift register 103, the data register 104, the level shifter 105 and the multiplexer 106 and the output circuit 107, had been added.

Attachment: Replacement Sheets

Annotated Sheet Showing Changes

REMARKS

Claims 1, 12 and 15 have been amended, claims 4-11 and 16-19 had been withdrawn from consideration, and no new claims are added. Thus, claims 1-3 and 12-15 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

In the Action dated December 14, 2006, the disclosure is objected to because there is an error in spelling on page 8, line 22. Since the specification had been amended with correction, Applicant believes that the objection is no longer applicable.

In the Action dated December 14, 2006, the drawings are objected to because the test input terminal is not connected with the shift register in Fig. 1 as claimed. Fig. 1 has been amended. In Fig. 1, previously omitted connection-line connected between the shift register 11 and the test signal input terminal 12 had been added. Further, previously omitted connection-lines connected among the shift register 103, the data register 104, the level shifter 105 and the multiplexer 106 and the output circuit 107 had been added.

As well as the amendment in Fig. 1, Figs. 3A and 4 had been amended. In these drawings, previously omitted connection-lines had been added. Since the drawings had been amended with corrections, Applicant believes that the objection is no longer applicable.

In the Action dated December 14, 2006, the claim 15 is objected to because of error in dependency. Since the claim 15 had been amended with corrections, Applicant believes that the objection is no longer applicable.

In the Action, Claims 1 and 3 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Imamura in view of Tsujii. The invention defined in independent claim 1 relates to a LSI chip having a test circuit. The characteristics of the invention claimed in claim 1 are,

(a) a single test signal input terminal, which receives a test signal, for testing the internal circuit,

(b) a single test signal output terminal, which outputs a test result only,

(c) a shift register, wherein

(i) output bits of the shift register is equal to a number of the output terminals of the LSI chip

(ii) a voltage level of one of the output bits of the shift register is different from these of other output bits of the shift register, and

(d) switches, the output terminals of the switches being commonly connected to the test signal output terminal.

Neither Imamura, Tsujii nor the combination discloses any of the above. The followings are detail explanation as to the differences between the invention and the cited references.

Characteristic (a): a single test signal input terminal

In the invention, the LSP chip includes an a single test signal input terminal, which receives a test signal, for testing an internal circuit,

On the other hand, Imamura discloses test signal input terminal 214 in Fig. 4. However, Applicant understands that the terminal 214 does not correspond to the single test signal input terminal of the invention. According to the disclosure of Imamura, the selection of the outputs from one of the functional device 202 and 203 and the test circuit 294 is made by the test signal, which is inputted to the terminal 214. Under the test operation, the outputs from the functional device 202 and 203 are blocked, and the output from the test circuit is outputted from the output terminals. It is clear from the drawings that the inputs of the test circuit are connected to the input terminals 208-213. Thus, the test circuit 204 does test the function of the signals inputted to the input terminals 208-213, not any functions of the functional device 202 and 203, which corresponds to the internal circuit of the invention. In other words, under the Imamura device, the test circuit 204 may test the wiring connection on the chip between the input terminals and the output terminals. Thus, if there is an error in the functional device 202 or 203, the test circuit 204 cannot detect the error. On the other hand, if there is an error in the internal circuit of the invention, the test circuit including the characteristics (a)~(d) described above can detect the error.

Thus, Applicant concludes that Imamura does not disclose the single test signal input terminal, which receives the test signal, for testing an internal circuit.

Characteristic (b): a single test signal output terminal

Imamura does not disclose the single test signal output terminal. The examiner asserted that the output terminal 218 corresponds to the ingle test signal

output terminal. **Applicant disagrees.** Under the normal operation (not in test mode) of Imamura, the output signal from functional device 202 or 203 is outputted from the output terminal 208. In other words, the output terminal 208 is not specialized for the test signal output. On the other hand, the single test signal output terminal of the invention outputs a test result **only**.

As the examiner understood from the specification in the Background of the Invention, the invention was made because of the difficulty for the test of the internal circuit by using the regular output terminal by the reason that the pitches between the output leads is disposed too closed. This was described in the specification on page 2 line18~page 3, line 6.Thus, the test signal output terminal 13 should be different from the regular output terminal O001-O284. However, the output terminal 208 of Imamura outputs the signal from the functional device 202 or 203, as well as the signal from the test circuit 204. Namely, Imamura does not disclosed any test specialized terminal.

Thus, Applicant concludes that Imamura does not disclose a single test signal output terminal, which outputs a test result only.

Characteristic (c): a shift register

As claimed, the invention includes a shift register, and the characteristic of the shift register of the invention includes that (i) the output bits of the shift register is equal to a number of the output terminals of the LSI chip, and (ii) the voltage level of one of the output bits of the shift register is different from these of other output bits of the shift register.

Imamura does not disclose any shift registers. The examiner asserted that the input/output buffer circuit 206 corresponds to the shift register of the invention.

However, **Applicant disagrees** because the voltage level of one of the output bits of the input/output buffer circuit 206 may be the same or may be the different from these of other output bits of the input/output buffer circuit 206. This totally depends on the voltage level of the input signals on the terminals 208-213 because the input/output buffer circuit 206 only consists of the inverters 222-234. No shift registrar's function exists in the input/output buffer circuit 206.

Characteristic (d): switches

Imamura does not disclose the switches. The examiner asserted that the clocked inverters 244 to 250 correspond to the switches of the invention. Applicant does not agree. The clocked inverters 244~250 are controlled all together by a signal from the inverter 251. In other words, the clocked inverters 244~250 cannot turn on/off individually. This is because the test signals on the lines connected to the clocked inverters 244~250 are used all together for the test under the test mode. It is meaningless under Imamura that one of the clocked inverters 244~250 turns on.

Applicant agrees the examiner's assertion in that Tsujii discloses a circuit responsive to a clock pulse. However, Tsujii discloses none of the above characteristics (a)~(d).

Therefore, since neither Imamura, Tsujii nor the combination does not disclose or suggest the claimed invention having the characteristics (a)~(d) described above, claim 1 clearly are not obvious by them, and is deemed to be clearly patentable, and the rejection of claim 1 accordingly should be withdrawn.

Further, claim 3 depends from claim 1 directly. Since Applicants believes that claim 1 includes a patentable subject matter, the rejection of claim 3 depended from claim 1 should be withdrawn.

In the Action, Claim 2 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Imamura and Tsuji in view of Tsujii. Claim 2 depends from claim 1 directly. Since Applicants believes that claim 1 includes a patentable subject matter, the rejection of claim 2 depended from claim 1 should be withdrawn.

In the Action, Claims 12 and 15 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Tsuji in view of Imamura. The invention defined in independent claim 12 relates to a chip carrier having following characteristics.

(e) input leads are extended in a first direction,

(f) output leads are extended in a second direction,

(g) a single test signal input lead is extended in the first direction, and the single test signal input lead receives a test signal for testing an internal circuit formed in the LSI chip, and

(h) a single test signal output lead is extended in the first direction, and the ingle test signal output lead outputting a test signal only.

Neither Tsujii, Imamura nor the combination discloses any of the above. The followings are detail explanation as to the differences between the invention and the cited references.

Initially, Applicant points out that Claim 12 is claimed for a particular layout of

some kinds of the leads. On the other hand, while Figs 1~4 may shows layouts of the components, it is clear that Fig. 1 of Tsujii does not disclose a layout rather a conceptual diagram of components. Thus, the Applicant understands that the layout claim cannot be rejected by the disclosure of the conceptual diagram of components shown in Tujii.

Characteristic (e): input leads

The examiner asserted that signal PADs 11~13, 16~18 correspond to the input leads. Applicant disagrees. The numbers 11~13, 16~18 of Tujii represent signal PADs, not leads. Thus, any of the signal PADs11~13, 16~18 does not extend to the first direction.

Characteristic (f): output leads

The examiner asserted that signal PADs 14, 19 correspond to the output leads. Applicant disagrees. The numbers 14, 19 of Tujii represent signal PADs, not leads. Thus, any of the signal PADs 14, 19 do not extend to the second direction.

Characteristic (g): a single test signal output lead

Applicant agrees the examiner's assertion that Tujii fails to disclose a single test input lead. But Applicant disagree the examiner's assertion in that Imamura discloses the single test output lead because of the reasons described above in the section (Characteristic (a)). In short, the test terminal 214 of Imamura does not receive a test signal for testing an internal circuit formed in the LSI chip.

Characteristic (h): a single test signal output lead

Applicant agrees the examiner's assertion that Tujii fails to disclose a single test output lead. But Applicant disagree the examiner's assertion in that Imamura discloses the single test output lead because of the reasons described above in the section (Characteristic (b)). In short, the output terminal 218 of Imamura is not a test signal specialized lead. In other words, the output terminal 218 of Imamura does not outputs a test signal only. In addition, while the single test signal output lead of the invention is extended in the first direction, the output terminal 218 of Imamura is extended in second direction.

Therefore, since neither Tujii, Imamura nor the combination does not disclose or suggest the claimed invention having the characteristics (e)~(h) described above, claim 12 clearly are not obvious by them, and is deemed to be clearly patentable, and the rejection of claim 12 accordingly should be withdrawn.

Further, claims 13~15 depend from claim 12 directly. Since Applicants believes that claim 12 includes a patentable subject matter, the rejection of claims 13~15 depended from claim 12 should be withdrawn.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any further fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Respectfully submitted,

Junichi Mimura (Reg. No. 40,351)
Oki America, Inc.
1101 14th Street N.W., Suite 555
Washington, D.C. 20005
Telephone: (202) 452-6190
Telefax: (202) 452-6148
Customer No.: 26071

June 1, 2007
Date

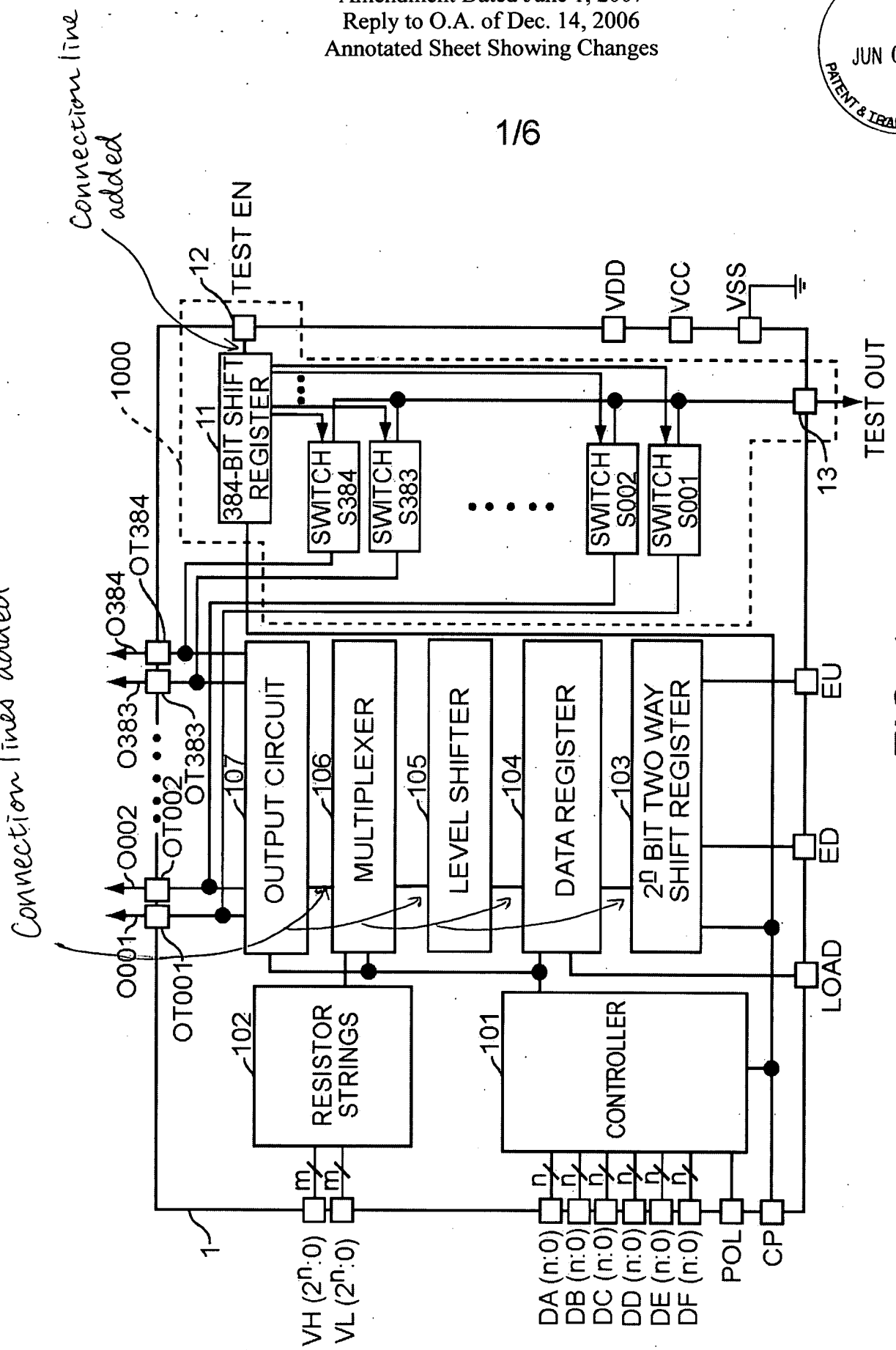

FIG. 1

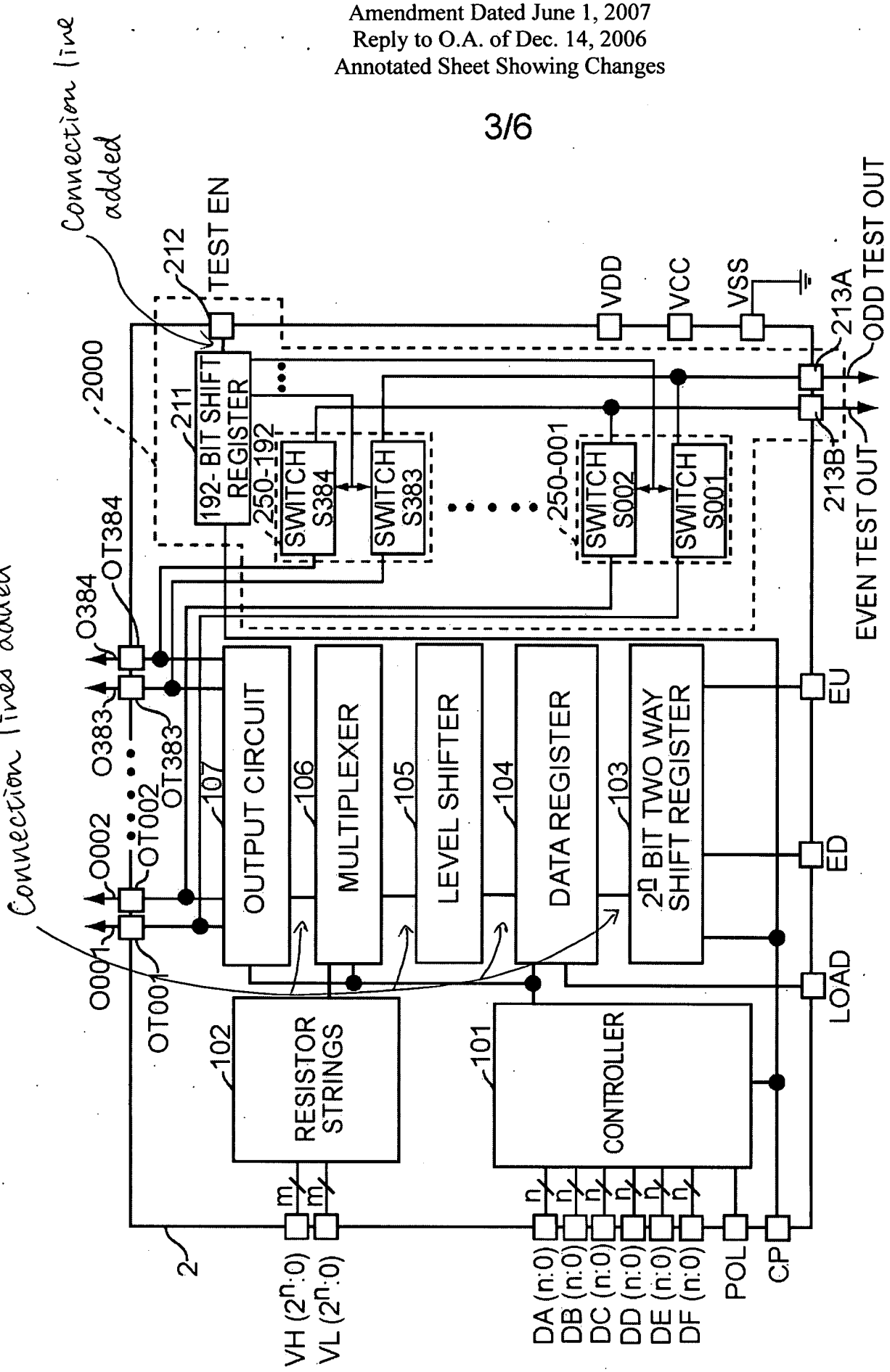
Connection line added
Connection lines added
2000
212
TEST EN
211
192- BIT SHIFT REGISTER
250-192
SWITCH S384
SWITCH S383
250-001
SWITCH S002
SWITCH S001
VDD
VCC
VSS
213A
ODD TEST OUT
213B
EVEN TEST OUT
O384
OT384
O383
OT383
O002
OT002
O001
OT001
107
OUTPUT CIRCUIT
106
MULTIPLEXER
105
LEVEL SHIFTER
104
DATA REGISTER
103
2n BIT TWO WAY SHIFT REGISTER
EU
ED
LOAD
102
RESISTOR STRINGS
101
CONTROLLER
m
m
n
n
n
n
n
n
2
VH (2n:0)
VL (2n:0)
DA (n:0)
DB (n:0)
DC (n:0)
DD (n:0)
DE (n:0)
DF (n:0)
POL
CP

FIG. 3A

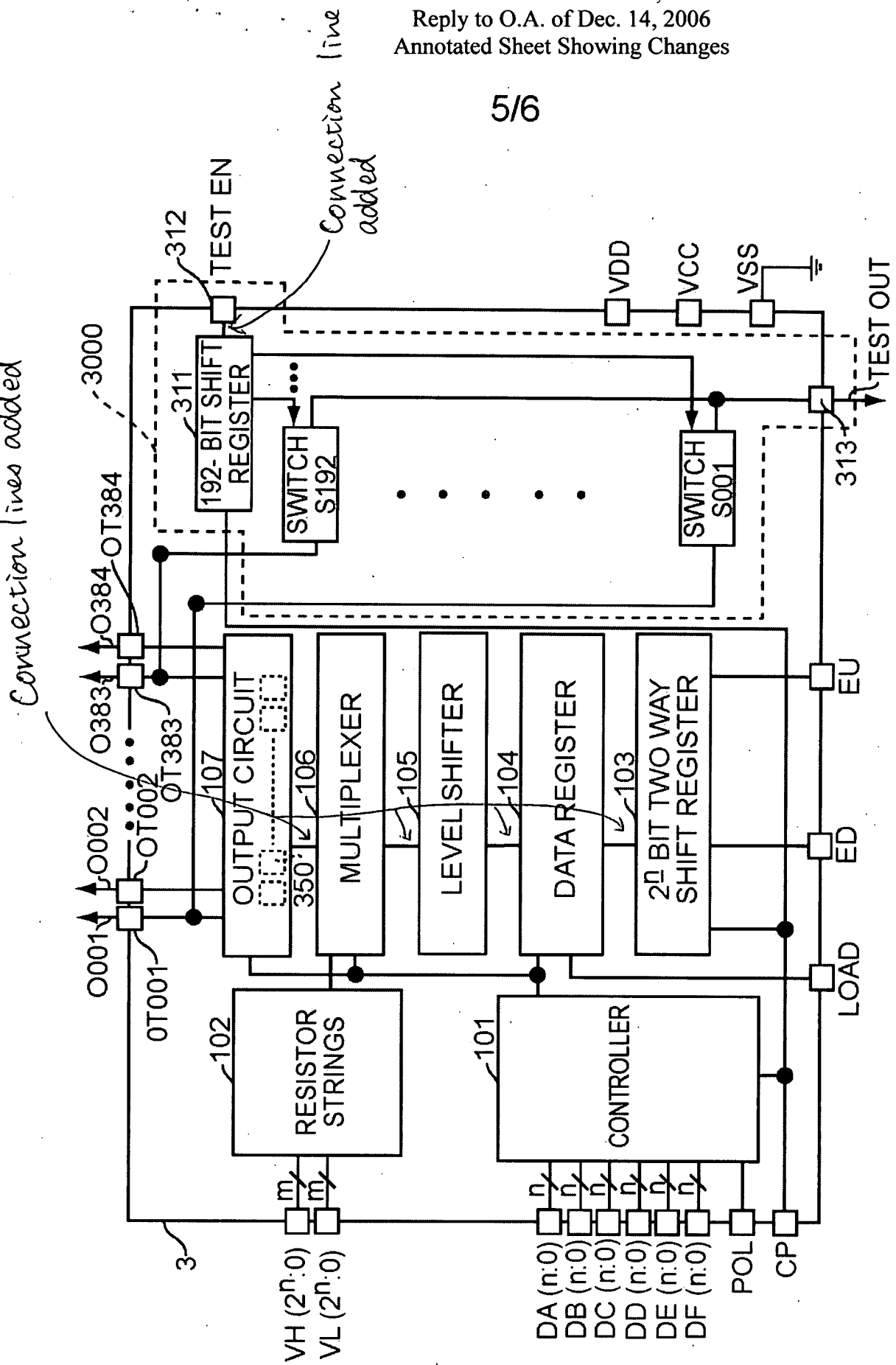
Connection line added
Connection lines added
TEST EN
312
3000
311
192- BIT SHIFT REGISTER
SWITCH S192
SWITCH S001
VDD
VCC
VSS
TEST OUT
313
OT384
O384
O383
OT383
OT002
O002
O001
OT001
107
OUTPUT CIRCUIT
350
106
MULTIPLEXER
105
LEVEL SHIFTER
104
DATA REGISTER
103
2n BIT TWO WAY SHIFT REGISTER
EU
ED
LOAD
102
RESISTOR STRINGS
101
CONTROLLER
m
m
n
n
n
n
n
n
3
VH (2n:0)
VL (2n:0)
DA (n:0)
DB (n:0)
DC (n:0)
DD (n:0)
DE (n:0)
DF (n:0)
POL
CP

FIG. 4